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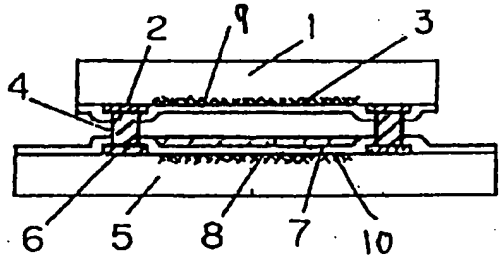
(54) Structure of chip on chip mounting preventing crosstalk noise

(57) The present invention is intended to solve a problem of crosstalk noise in a so-called system module, which occurs as a result of interference between signals running in each of respective wiring layers of a first semiconductor chip and a second semiconductor chip stacked surface to surface with a small gap, and invites malfunctioning of semiconductor devices. As shown in Fig.1, the semiconductor device comprises a first semiconductor chip 1 having a first electrode pad 2 and a first wiring layer 9 in the main surface, a second semiconductor chip 5 having a second electrode pad 6 located at a corresponding place and a second wiring layer 10 in the main surface facing to the first semiconductor chip, a bump 4 for electrically coupling first electrode pad 2 and second electrode pad 6 together, an insulation layer 8 disposed between the main surfaces of first semiconductor chip 1 and second semiconductor chip 5 facing to each other, and an electro-conductive layer 7 disposed between the main surfaces of first semiconductor chip and second semiconductor chip facing to each other.

F I G. 1



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Description

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor devices which are assembled as multichip module or the like, in the field of electronic components mounting.

To meet the demand for making electronic appliances smaller, providing higher functions and higher operating speed, an effort is being made to put plurality of electronic components into one unit to form a module. As a so-called multichip module, it has been proposed to mount a semiconductor chip on other semiconductor chip and house together in a single encapsulation to be mounted on a printed circuit board.

In the following, explanation is made on a conventional semiconductor device in which plural semiconductor chips are stacked. Fig. 18 shows a cross sectional structure of the conventional semiconductor device, Fig.19 the process steps of coupling the chips.

In a conventional structure, a first semiconductor chip 91 having a first electrode pad 92 and a passivation layer 94 is mounted on a second semiconductor chip 96 having a second electrode pad 97 and a passivation layer 99. The first electrode pad 92 is coupled with the second electrode pad 97 via barrier metals 93 and 98, each formed on the respective electrode, by means of the flip chip mounting method using a metal bump 95 comprised of a solder. In a case when forming the bump 95 by electroplating, normally barrier metals 93 and 98 are disposed between bump 95 and each of first electrode pad 92 and second electrode pad 97, in order to ensure contact between bump 95 and these electrode pads 92, 97. Furthermore, the gap between first semiconductor chip 91 and second semiconductor chip 96 is filled with an insulation resin 100 of epoxy group, acrylic group or silicone group.

Next, explanation is made on a process to couple first semiconductor chip 91 with second semiconductor chip 96. As shown in process (a) of Fig.19, a barrier metal layer 93 of Ti, Pd or Au is formed by the EB evaporation method or the like. Then, the surface is covered with a photo resist 101 using the technology of photolithography, excluding an area of first electrode pad 92, as shown in process (b). Then, as shown in process (c), Pb or Sn solder which is to become bump 95 is formed on barrier metal layer 93 above electrode pad 92 by means of electroplating or the like. After removing photo resist 101, barrier metal layer 93 is etched off with aqua regia, fluoric acid, etc. leaving an area above the electrode pad, process (d). Barrier metal 98 is formed also on second semiconductor chip 96 by the same process.

Next, as shown in process (e), bump 95 of first semiconductor chip 91 is aligned to barrier metal 93 of second semiconductor chip 96, and then the two are coupled together by heating or by pressing. Then, as shown in process (f), insulation resin 100 is provided between first semiconductor chip 91 and second semiconductor chip 96, and cured; thus the mounting of first semiconductor chip 91 on second semiconductor chip 96 is completed.

In the conventional structure as explained above, however, the occurrence of crosstalk noise is inevitable because of interference between signals flowing in the wiring layer formed on the main surface of each respective semiconductor chip, if the gap between first semiconductor chip and second semiconductor chip is to be made narrower than 100μm.

In order to suppress the size of crosstalk noise signal within 10% of that of the source signal, it has been reported that two semiconductor chips need to be separated by more than 300μm even when the two are placed horizontally side by side. Therefore, when stacking two semiconductor chips vertically a gap of more than several hundreds um seems to be necessary; to narrow the gap to be less than 100μm has been a hard task to attain.

SUMMARY OF THE INVENTION

The present invention aims to present a semiconductor device wherein the occurrence of crosstalk noise between a wiring layer of a first semiconductor device and a wiring layer of a second semiconductor device is reduced, and a manufacturing method thereof.

A semiconductor device according to an embodiment of the present invention comprises a first semiconductor chip having a first electrode pad and a first wiring layer on the main surface, a second semiconductor chip having a second electrode pad located at a corresponding place and a second wiring layer on the main surface facing to the first semiconductor chip, a connecting member for electrically coupling the first electrode pad with the second electrode pad, an insulation member disposed between the main surfaces of first semiconductor chip and second semiconductor chip facing to each other, and an electro-conductive member disposed between the main surfaces of first semiconductor chip and second semiconductor chip facing to each other.

A semiconductor device manufacturing method according to an embodiment of the present invention comprises a process to dispose a first semiconductor chip and a second semiconductor chip with their main surfaces facing to each other, a process to dispose an insulation member between the first semiconductor chip and the second semiconductor chip, a process to dispose an electro-conductive member between the first semiconductor chip and the second semiconductor chip, and a process to electrically couple a first electrode pad and a second electrode pad with a connecting member.

In the above described constitution, the crosstalk noise which occurs between the wiring layers can be significantly reduced even when the layers are placed close to each other, as an electro-conductive member is disposed between the first semiconductor chip and the second semiconductor chip. For example, even if the

gap between first semiconductor chip and second semiconductor is narrowed to be less than 100μm, the value of crosstalk noise can be suppressed within 10% of the value of source signal.

A semiconductor device according to other embodiment of the present invention is comprised of a first semiconductor chip having a first eletrode pad, a first wiring layer and a first elements region on the main surface; and a second semiconductor chip having a second electrode pad located at a corresponding place, a second wiring layer and a second elements region on the main surface facing to the first semiconductor chip; wherein the second semiconductor chip has a larger chip area than that of the first semiconductor chip, and the second wiring layer and the second elements region are formed in an area where they do not face the first wiring layer and the first elements region. In this constitution, the occurrence of crosstalk noise is suppressed as the wiring layer and the elements region of each chip are disposed so as not to face to each other.

A semiconductor device according to another embodiment of the present invention is comprised of a first semiconductor chip and a second semiconductor chip disposed with their main surfaces facing to each other, wherein a wiring of a first wiring layer formed in the first semiconductor chip and a wiring of a second wiring layer formed in the second semiconductor chip are disposed in a state crossing to each other without having contact, viz. crossing at right angle or some other angle to each other. By disposing the two wirings so as not to form a parallel arrangement, the crosstalk noise becomes difficult to occur. Thus, the crosstalk noise can be reduced to a level low enough not to cause an erroneous operation of a semiconductor device.

A semiconductor device according to a further diverse embodiment of the present invention is comprised of a first semiconductor chip and a second semiconductor chip disposed with their main surfaces facing to each other, wherein the difference between the driving voltage of the first semiconductor chip and that of the second semiconductor chip has a smaller value than threshold voltage, which determines the ON or OFF, of a semiconductor chip whose driving voltage is lower of the two. Thus, the crosstalk noise can be suppressed also by making the difference of driving voltages between the two chips smaller than threshold voltage value of either one of the chips the driving voltage of which is lower.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a cross sectional view of a semiconductor device according to a first embodiment of the present invention.

Fig.2 shows a top view of a second semiconductor chip of the first embodiment.

Fig.3 shows process steps of a first semiconductor device manufacturing method of the semiconductor device according to the first embodiment of the present invention.

Fig.4 shows process steps of a second semiconductor device manufacturing method of the semiconductor device according to the first embodiment.

Fig.5 shows a cross sectional view of a semiconductor device according to a second embodiment of the present invention.

Fig.6 shows a top view of a second semiconductor chip of the second embodiment.

Fig.7 shows process steps of a semiconductor device manufacturing method of the semiconductor device according to the second embodiment.

Fig.8 shows a cross sectional view of a semiconductor device according to a third embodiment of the present invention.

Fig.9 shows process steps of a semiconductor device manufacturing method of the semiconductor device according to the third embodiment.

Fig.10 shows a cross sectional view of a semiconductor device according to a fourth embodiment of the present invention.

Fig.11 shows process steps of a semiconductor device manufacturing method of the semiconductor device according to the fourth embodiment.

Fig.12 shows a cross sectional view of a semiconductor device according to a fifth embodiment of the present invention.

Fig.13 shows a cross sectional view of a semiconductor device according to a sixth embodiment of the present invention.

Fig.14 shows a see-through plan view of a semiconductor device according to a seventh embodiment.

Fig.15(a) shows an outline concept of a semiconductor device according to an eighth embodiment of the present invention; Fig.15(b) an equivalent circuit diagram between the wirings of the semiconductor device.

Fig.16 is a characteristics chart showing the relationship of signal waveforms when different driving voltages are applied on a first semiconductor chip and a second semiconductor chip in a comparative case.

Fig.17 is a characteristics chart showing the relationship of signal waveforms when a same driving voltage is applied on a first semiconductor chip and a second semiconductor chip of the eighth embodiment of the present invention.

Fig.18 shows a cross sectional view of a prior art semiconductor device.

Fig.19 shows process steps of a prior art semiconductor device manufacturing method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, embodiments of the present invention are described referring to Figs.

(embodiment 1)

Fig.1 shows structure of coupling semiconductor chips in a semiconductor device according to a first embodiment of the present invention. The semiconductor device comprises a first semiconductor chip 1 having a first electrode pad 2, a first wiring layer 9 and a passivation layer 3 covering the surface excluding the first electrode pad 2; and a second semiconductor chip 5 having a second electrode pad 6, on which chip the first semiconductor chip is mounted. On second semiconductor chip 5, an insulation layer 8 is formed to cover the surface except second electrode pad 6, and an electro-conductive layer 7 is formed above insulation layer 8 to cover an area corresponding to a second wiring layer 10. First electrode pad 2 and second electrode pad 6 are electrically coupled together by a bump 4 constituting an extruding electrode. When encapsulating the semiconductor device, the gap between first semiconductor chip 1 and second semiconductor chip 5 may be filled, whenever necessary, with an insulation resin of epoxy group, acrylic group or silicone group. For instance, when mounting the semiconductor device in the bare chip state on a printed circuit board, fill in an insulation resin between the semiconductor chips 1 and 5. When encapsulating with a lead frame, insert the semiconductor device within a mold and then pour an insulation resin into the mold.

Fig.2 shows arrangement of second electrode pads 6 and electro-conductive layer 7 on second semiconductor chip 5. Electro-conductive layer 7 has an extended area or a ground terminal 11 which is coupled with one of second electrode pads 6. The ground terminal 11 is not a must; however, it is recommended to form a ground terminal 11, and the effect of reducing cross-talk noise is ensured by grounding the terminal 11.

Electro-conductive layer 7 may be formed on passivation layer 3, instead of on insulation layer 8; or on both insulation layer 8 and passivation layer 3. What is required for electro-conductive layer 7 is to cover at least first wiring layer 9 and second wiring layer 10.

Fig.3 shows a method of coupling a first semiconductor chip 1 and a second semiconductor chip 5 together.

In the first place, an electro-conductive film 12 of an Al-Si-Cu alloy is formed on insulation layer 8 by sputtering, as shown in process (a). Then, in order to obtain an electro-conductive layer 7 having a shape shown in Fig.2, unnecessary part of electro-conductive film 12 is removed by dry-etching, after covering the opening of a second electrode pad 6, which is to make itself a ground terminal 11, and an area above wiring layer 10 with a photo resist, process (b). In a case when ground terminal 11 is not needed, it may be removed.

As to material for the electro-conductive film 12, because of a fact that the wiring is comprised of an Al-Si-Cu alloy, use of the same material is advantageous in manufacturing. However, the electro-conductive film 12 is not limited to the material; other electro-conductive material may be used.

Next, as shown in process (c), a bump 4 or a metal extrusion of e.g. Ni-core Au bump is formed by electroless plating on first electrode pad 2 of first semiconductor chip 1. And then, first semiconductor chip 1 and second semiconductor chip 5 are disposed so as bump 4 and second electrode pad 6 face to each other, as shown in process (d). And, as shown in process (e), first semiconductor chip 1 and second semiconductor chip 5 are pressed together and heated by a pressing/heating jig 13. Pressure then is within a range from 0.1g to 100g per one bump; heating temperature is within a range from 250°C to 450°C. By the pressing/heating, the Au-Al alloy junction is formed. In the case of Au-Au junction, viz. when Ni-core Au bump is formed on both of electrode pads 2, 6, or when second electrode pad 6 is coated with Au, the pressing/heating conditions remain the same as in the case of Au-Al alloy junction. Conditions for the case of solder alloy junction are: heating temperature from 60°C upto 250°C; pressure from the self weight of first semiconductor chip 1 upto several grams. Besides these alloy junction methods, the flip chip method such as **MBB**(micro bump bonding) method, well known as **COG**(chip on glass) method, wherein junction is made via insulation resin, may be used.

As described above, a semiconductor device according to this embodiment comprises two semiconductor chips (first semiconductor chip and second semiconductor chip) coupled via metal extrusion, and an electro-conductive layer 7 disposed between said two semiconductor chips. Therefore, the crosstalk noise is reduced. As the electro-conductive layer 7 can be formed during the process steps of a conventional semiconductor device manufacturing method, there is no need of introducing an additional production facility.

Fig.4 shows another coupling method, wherein the method of forming electro-conductive layer is different from that of Fig. 3. In the first place, as shown in process (a) of Fig.4, all of the electrode pads 6, excluding the one to be connected to ground terminal 11, are covered with photo resist 14. Next, as shown in process (b), electro-conductive film 12 composed of Sn/Pd/Ni three layers is formed by electroless plating over insulation layer 8. Photo resist 14 is removed, and then conductive film 12 is there. The conductive film 12 is utilized as it is as the electro-conductive layer. The succeeding processes (c), (d) and (e) are the same as (c), (d) and (e) processes of Fig.3. What are different from the case of Fig.3 are that the conductive layer 12 is formed by the electroless plating and that the conductive layer 12 is provided not only in an area above second wiring layer 10, but also to cover an area surrounding second electrode pads 6. As to electro-conductive layer 12, those which can be plated through electroless plating, e.g. Ag or Sn metal layer, or Sn/Pd two layers or the like may be used, besides said Sn/Pd/Ni layers. Also, Sn-Pd or Sn-Pd-Ni alloy layer obtained by heating these two or three

layers may be used. Further, it is not essential for the electro-conductive layer 12 to be formed to cover the entire surface excluding second electrode pads 6; the electro-conductive layer may be formed for an area covering at least first wiring layer 9 and second wiring layer 10.

The coupling method as shown in Fig.4 does not require the electro-conductive layer be formed during manufacturing process of a semiconductor device. Therefore, the electro-conductive layer can be formed at ease on any finished bare chips if there is a facility available for electroless plating.

Although the coupling methods of Fig.3 and Fig.4 exemplified a Ni-core Au bump for the bump 4, an Au bump, a solder bump consisting of Sn-Pb alloy, In-Sn alloy, etc. may of course be used. Besides the above, a transfer bump method may be employed. Diameter of the Ni-core Au bump and Au bump is from 5μm upto 100μm, the solder bump approximately 100μm. If the gap between electrode pads 2 and 6 are to be made larger in order to further reduce the crosstalk noise, it is recommended to form a bump also on electrode pad 6 of second semiconductor chip 5. In this case, second semiconductor chip 5 undergoes the process (c), in advance to processes (a) and (b).

(embodiment 2)

Fig.5 shows a cross sectional structure of a semiconductor device according to a second embodiment of the present invention. The constituent components in Fig.5 having the same functions as those in Fig.1 are indicated by the same symbols, and explanations to which are omitted. In the semiconductor device of Fig.5, an insulation film 16 carrying an electro-conductive layer 18 is disposed between first semiconductor chip 1 and second semiconductor chip 5. First electrode pad 2 and second electrode pad 6 are coupled, via bumps 4a, 4b, by a metal extrusion 17 formed on insulation film 16.

Fig.6 is a plan view showing the arrangement of metal extrusions 17 formed on insulation film 16 and electro-conductive layer 18. Symbol 19 denotes a metal extrusion to be connected to the ground terminal, among metal extrusions 17 formed on insulation film 16.

Fig.7 shows process steps of an exemplary method for coupling semiconductor chips of the semiconductor device. In the first place, an insulation resin 20 of acrylic group, epoxy group or silicone group is applied on second semiconductor chip 5, as shown in process (a). Then, as shown in process (b), a polyimide insulation film 16 having a metal extrusion 17 of Au and an electro-conductive layer 18 is disposed with the position aligned on insulation resin 20. Besides Au, metals such as a Ni-core Au, or Sn-Pb, In-Sn solder or the like may be used as the metal extrusion 17. Or, in place of the metal extrusion 17, an electro-conductive extrusion comprising of a paste containing electro-conductive filler or the like may be used depending on situation. However, as the electro-conductive extrusion has a higher electrical resistance than the metal extrusion, the latter is preferred.

Then, as shown in process (c), an insulation resin 22 of acrylic group, epoxy group or silicone group is applied on insulation film 16. First semiconductor chip 1 is disposed on insulation resin 22 aligning bump 4a formed on electrode pad 2 with metal extrusion 17 on insulation film 16, as shown in process (d). And then, first semiconductor chip 1 and second semiconductor chip 5 are coupled together by the same method and conditions of pressing/heating as in process (e) of Fig.3. In a case when insulation film 16 is consisted of polyethylene or the like whose heat-resisting property is inferior to polyimide, and metal extrusion 17 is consisted of a low temperature solder of Sn-In group solderable at a temperature of several tens degree C, first semiconductor chip 1 is mounted on second semiconductor chip 5 by performing the solder alloy junction, at the same time curing insulation resins 20 and 22. If insulation resins 20 and 22 are of a light-curing type insulation resin, first semiconductor chip 1 may be mounted on second semiconductor chip 5 with a pressing/heating tool 13 irradiating ultraviolet rays, thus curing the insulation resins 20 and 22 while pressing first semiconductor chip 1 and second semiconductor chip 5 together. If extrusion 17 is comprised of a paste containing electro-conductive filler, first semiconductor chip 1 is mounted on second semiconductor chip 5 by using a light-curing type insulation resin for the insulation resins 20 and 22, with pressing/heating tool 13 irradiating ultraviolet rays, thus curing insulation resins 20 and 22 while pressing first semiconductor chip 1 and second semiconductor chip 5 together.

In this embodiment, as an electro-conductive layer 18 provided on insulation film 16 is disposed between first semiconductor chip 1 and second semiconductor chip 5, the crosstalk noise can be significantly reduced. Further, as the metal extrusion can be formed in advance on an insulation film by a process apart from the manufacturing process of semiconductor chip itself, the embodiment is advatageous in volume production.

The ground terminal is formed on either first semiconductor chip or second semiconductor chip in the embodiment. The ground terminal may of course be formed on an external circuit. And the same effect is obtained by connecting the terminal with electro-conductive layer 18.

(embodiment 3)

Fig.8 shows a cross sectional structure of a semiconductor device according to a third embodiment of the present invention. The constituent components in Fig.8 having the same functions as those in Fig.1 are given with the same symbols, and explanations to which are omitted. The semiconductor device of Fig.8 comprises an electro-conductive foil 23 of copper buried in an insulation resin 24, 25, disposed between first semiconductor chip 1 and second semiconductor chip 5. In

place of the copper foil, an aluminum foil or other electro-conductive metal foil may be used as the electro-conductive foil 23.

Fig.9 shows process steps of a method for coupling semiconductor chips of the semiconductor device. In the first place, a bump 4a of Ni-core Au bump is formed by electroless plating on first electrode pad 2 of first semiconductor chip 1, as shown in process (a). A bump 4b is likewise formed on second electrode pad 6 of second semiconductor chip 5. Besides the Ni-core Au bump, Au or other metal, or solders such as Sn-Pb, In-Sn, etc. may be used for the bump 4a, 4b. Diameter of bumps 4a, 4b is: from 5μm upto 100μm for Ni-core Au bumps and Au bumps; approximately 100μm for solder bumps.

Next, as shown in process (b), an insulation resin 24 of acrylic group, epoxy group or silicone group is applied on a passivation layer 3. Then, as shown in process (c), electro-conductive foil 23 of copper having a shape covering the surface of first semiconductor chip 1 excluding an area of bump 4a is disposed on insulation resin 24. An insulation resin 25 of acrylic group, epoxy group or silicone group is then applied on electro-conductive foil 23, as shown in process (d).

Then, as shown in process (e), bump 4a is aligned with bump 4b. Using a pressing/heating tool 13, first semiconductor chip 1 and second semiconductor chip 5 are pressed together with a pressure from 0.1g upto 100g per one bump, and heated at a temperature approximately from 250°C upto 450°C to perform the Au-Au junction. In the case of Au-Al alloy junction, where a bump is formed on either one of the semiconductor chips 1, 5, the pressing/heating conditions remain the same as in said case of Au-Au junction. For the solder alloy junction, the temperature range is from 60°C upto 250°C, the pressure is from the self weight of semiconductor chip 5 itself upto several grams. In the mean time, insulation resins 24, 25 are simultaneously cured, and second semiconductor chip 5 is coupled on first semiconductor chip 1. If the insulation resins 24, 25 are a light-curing type insulation resin, second semiconductor chip 5 can be mounted on first semiconductor chip 1 with pressing/heating tool 13 irradiating ultraviolet rays, thus the insulation resins 24, 25 are cured while first semiconductor chip 1 and second semiconductor chip 5 are pressed together.

As described above, as the semiconductor device of the present embodiment comprises an electro-conductive foil disposed between two semiconductor chips coupled together by utilizing a metal extrusion, the crosstalk noise that arise between first wiring layer 9 and second wiring layer 10 can be reduced. By disposing an electro-conductive foil in place of an electro-conductive layer employed in the above described embodiments 1 and 2, the present embodiment provides an effect of crosstalk noise reduction at an easier way as compared with said embodiments 1, 2.

(embodiment 4)

Fig.10 shows a cross sectional structure at the coupling part of semiconductor chips of a semiconductor device according to a fourth embodiment of the present invention. A first semiconductor chip 31 comprises a first electrode pad 32, a first passivation layer 33 and a first elements region 34 containing wiring layer. A second semiconductor chip 35 has a chip size larger than first semiconductor chip 31, and comprises a second electrode pad 36, a second passivation layer 37, a second elements region 38 containing wiring layer, and a pad 36a for connection with an external circuit. Where, second elements region 38 is formed in an area not facing to first semiconductor chip 31. First electrode pad 32 and second electrode pad 36 are electrically connected together by means of a metal extrusion, or a bump 39. The gap between first semiconductor chip 31 and second semiconductor chip 35 including their vicinities are filled with an insulation resin 40. The insulation resin 40 is not an essential component, but it may be used whenever necessary.

Fig.11 shows process steps of mounting two semiconductor chips of the semiconductor device.

In the first place, as shown in process (a), a bump 39 of Ni-core Au is formed by electroless plating on electrode pad 32 of first semiconductor chip 31. Bump 39 may be either an Au bump, or a solder bump comprising of Sn-Pb, In-Sn, etc. It may be formed also by a transfer bump method. The diameter of bump 39 is: from 5μm upto 100μm for Ni-core Au bumps and Au bumps; approximately 100μm for solder bumps. Bump 39 may be formed on both first semiconductor chip 31 and second semiconductor chip 35.

Next, as shown in process (b), first electrode pad 32 is aligned with second electrode pad 36 via bump 39. Then, first semiconductor chip 31 is mounted on second semiconcuctor chip 35 using a pressing/heating tool 13. When, the chips are pressed together with a pressure from 0.1g upto 100g per one bump, at a temperature within a range from 60°C to 250°C to perform the Au-Al alloy junction. In the case of Au-Au junction, the pressing/heating conditions remain the same as in the Au-Al alloy junction. In a case of the solder alloy junction, the heating temperature is within a range from 60°C to 250°C, the pressure is from the weight of semiconductor chip itself upto several grams. Besides the alloy junction method, a flip chip method such as **MBB**(micro bump bonding) method well known as **COG** method, wherein the coupling is performed via an insulation resin, may be used.

Then, as process (d) shows, the gap between first semiconductor chip 31 and second semiconductor chip 35 and their vicinities are filled with an insulation resin 40, and cured. If the insulation resin 40 is a light-curing type insulation resin, second semiconductor chip 35 may be mounted on first semiconductor chip 31 irradiating ultraviolet rays, thus insulation resin is cured while first semiconductor chip 31 and second semiconductor

chip 35 are pressed together by pressing/heating tool 13.

As described above, as there is no second elements region 38, including the wiring layer, in an area beneath first elements region 34, the occurrence of crosstalk noise between first elements region 34 and second elements region 38 is suppressed.

(embodiment 5)

A fifth embodiment of the present invention as shown in Fig.12 is a modification of the fourth embodiment shown in Fig.10; an **EPROM**(erasable programmable read-only memory) module comprised of a second semiconductor chip 42 containing memory circuits and logic circuits, and a first semiconductor chip 41, which comprises a general-use **MCU**(micro-computer), mounted on the second semiconductor chip 42. The constituent components in Fig.12 having the same functions as those of Fig.10 are given with the same symbols, and explanations to which are omitted. An **EPROM** 43 and a logic circuit 44 are formed in an area not facing to second semiconductor chip 42. The logic circuit 44 may contain other memories. Also in this embodiment, an insulation resin 40 may be filled in, wherever necessary, as shown in Fig.10.

The method of coupling first semiconductor chip 41 and second semiconductor chip 42 together remains the same as that of Fig.11, processes (a) - (c); therefore explanation of which is omitted.

In this embodiment, as the **EPROM** 43 and logic circuit 44 are formed in an area of second semiconductor chip 42 not facing to the first semiconductor chip 41, the occurrence of crosstalk noise is suppressed even without providing an electro-conductive layer. Furthermore, different from a conventional semiconductor device wherein an **EPROM** is formed beneath first semiconductor chip, the **EPROM** 43 of this embodiment is placed with its surface open to upward; therefore, programs and data stored in **EPROM** 43 can be erased at ease by irradiating ultraviolet rays from the upward, and rewritten. In a case where at least **EPROM** 43 is located not overlaid by first semiconductor chip 41, the erasing by ultraviolet rays is possible. In a case where logic circuit 44 is formed beneath first semiconductor chip 41, the occurrence of crosstalk noise can be suppressed by disposing an electro-conductive layer between first semiconductor chip 41 and second semiconductor chip 42.

(embodiment 6)

A sixth embodiment of the present invention shown in Fig.13 is another modification of the fourth embodiment as shown in Fig.10; an **ICE**(in-circuit emulator) module comprising a second semiconductor chip 46 comprised of an **ICE** chip, and a first semiconductor chip 45 comprised of a general-use **MCU** (micro-computer) which is mounted on the second semiconductor chip 46. The constituent components of Fig.13 having the same functions as those in Fig.10 are given with the same symbols, and explanations to which are omitted. A circuit 47 comprised of an **ICE** circuit and a memory is formed on second semiconductor chip 46 in an area not facing to first semiconductor chip 45. A pad 36a is a user external pad; the total number of pads 36 plus pad 36a is larger than the number of first electrode pads 32. The circuit 47 is formed so as the square measure of circuit 47 is smaller than the area of second semiconductor chip 46 minus area of the general-use **MCU**.

Method of coupling first semiconductor chip 45 and second semiconductor chip 46 together remains the same as that shown in Fig.11, processes (a) through (c); therefore explanation to which is omitted.

The occurrence of crosstalk noise is suppressed also in this embodiment because the circuit 47 comprising of **ICE** circuit and memory is formed on second semiconductor chip 46 in an area not facing to first semiconductor chip 45.

(embodiment 7)

Fig.14 is a see-through plan view of a semiconductor device according to a seventh embodiment of the present invention, as viewed from above a first semiconductor chip 51. On the first semiconductor chip 51, a first electrode pad 52 and a first wiring 53 are formed. On a second semiconductor chip 55, a second electrode pad 56 and a second wiring 57 are formed. The first semiconductor chip 51 and the second semiconductor chip 55 are positioned in a manner so that the direction of wiring 53 and the direction of wiring 57 form approximately right angle. First electrode pad 52 and second electrode pad 56 are coupled by a metal extrusion, or a bump 54. The gap between first semiconductor chip 51 and second semiconductor chip 55, and their vicinities are filled with an insulation resin 58. The insulation resin 58 is not an essential member, it may be provided whenever needed.

Method of coupling first semiconductor chip 51 and second semiconductor chip 55 together remains the same as that of Fig.11, processes (a) through (d); therefore explanation to which is omitted.

Thus, the crosstalk noise that occurs between wiring 53 and wiring 57 is significantly reduced by arranging the positioning of first semiconductor chip 51 and second semiconductor chip 55 so as the direction of wiring 53 and the direction of wiring 57 cross at approximately right angle to each other. The crosstalk noise increases along with deviation of the crossing angle of the directions of wiring 53 and wiring 57 from the right angle. Therefore, it is most preferred to have the direction of wiring 53 and the direction of wiring 57 cross at approximately right angle. However, it is not the intention of the present invention to limit the positioning arrangement to the right angle, but the crossing angle between the direction of wiring 53 and the direction of wiring 57 may be made smaller than the right angle in

so far as the level of crosstalk noise is lower than a level at which a functional error is induced on the semiconductor device. When directions of the two wirings are in parallel to each other the crosstalk noise reaches its peak; therefore, such an arrangement is the least preferred.

(embodiment 8)

Fig.15(a) is a conceptual drawing showing the cross section and the circuit of a semiconductor device according to an eighth embodiment of the present invention. On a first semiconductor chip 61, a first electrode pad 62 and a first wiring 63 are formed. On a second semiconductor chip 65, a second electrode pad 66 and a second wiring 67 are formed. The first electrode pad 63 and the second electrode pad 66 are coupled together via a metal extrusion, or a bump 64, so as first wiring 63 and second wiring 67 do not touch to each other. Method of coupling first semiconductor chip 61 and second semiconductor chip 65 remains the same as that of Fig.11, processes (a) through (c); therefore explanation to which is omitted.

Fig.15(b) shows an equivalent circuit diagram, where each length of first wiring 63 and second wiring 67 is 1mm, and wiring 63 and wiring 67 are in parallel to each other. In Fig.15(b) shows a resistance 68, an inductance 69 and a capacitance 70 against substrate of first wiring 63; a resistance 71, an inductance 72 and a capacitance 73 against substrate of second wiring 67; and a mutual inductance 74 and a mutual capacitance 75 between wiring 63 and wiring 67.

In this embodiment, in order to suppress the crosstalk noise induced by mutual inductance 74 and mutual capacitance 75, the difference between driving voltage of first semiconductor chip 61 and driving voltage of second semiconductor chip 65 is made to be smaller than threshold voltage of either one of the semiconductor chips the driving voltage of which is lower. For example, assuming the driving voltage of second semiconductor chip 65 to be 2V, and the ON and OFF is determined at 1V as the border, the driving voltage of first semiconductor chip 61 is set to be under 3V. In this case, the difference between the two driving voltages becomes under 1V, or smaller than the threshold voltage 1V; therefore the crosstalk noise diminishes.

For the purpose of comparison, Fig.16 shows the occurrence of crosstalk noise Q3 immediately before each respective input buffer; where driving voltage Q2 of second semiconductor chip 65 is 2V, and driving voltage Q1 of first semiconductor chip 61 is 5V. In this case, the difference between the driving voltages is 3V, or larger than the lower driving voltage Q2 and evidently higher than the threshold value; therefore, it is seen that a substantial crosstalk noise Q3 is induced on wiring 67 of second semiconductor chip 65.

As a practical example of this embodiment, Fig.17 shows the occurrence of crosstalk noise Q6 immediately before each respective input buffer; where driving voltage Q4 of first semiconductor chip 61 and driving voltage Q5 of second semiconductor chip 65 are both 3.3V. In this case, the difference between the driving voltages is 0V, or evidently smaller than the threshold value; therefore, it is seen that the level of crosstalk noise Q6 is too low to give influence on operation of the semiconductor device.

As described above, in a constitution where first semiconductor chip 61 and second semiconductor chip 65 are disposed facing to each other, and electrially coupled via bump 64, the crosstalk noise that occurs between the wirings of first semiconductor chip 61 and second semiconductor chip 65 can be reduced to a level not to cause an erroneous operation of semiconductor device, if the difference between driving voltage of first semiconductor chip 61 and driving voltage of second semiconductor chip 65 is smaller than thershold voltage of either one of the semiconductor chips the driving voltage of which is lower.

Although the present invention has been described in terms of the presently preferred embodiments, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become possible. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

Claims

1. A semiconductor device comprising:

   a first semiconductor chip having a first electrode pad and a first wiring layer disposed in the main surface;
   a second semiconductor chip having a second electrode pad located at a corresponding place and a second wiring layer disposed in the main surface facing to said first semiconductor chip;
   a coupling member for electrically coupling said first electrode pad and said second electrode pad together;
   an insulation member disposed between said main surfaces, facing to each other, of said first semiconductor chip and said second semiconductor chip; and
   an electro-conductive member disposed between said main surfaces, facing to each other, of said first semiconductor chip and said second semiconductor chip.

2. The semiconductor device of claim 1, wherein

   said insulation member is comprised of an insulation layer formed on at least one of said main surfaces of said first semiconductor chip and said second semiconductor chip, and

said electro-conductive member is comprised of an electro-conductive layer formed on said insulation layer.

3. The semiconductor device of claim 1, wherein

said insulation member is comprised of an insulation film having said coupling member in the circumference, and
said electro-conductive member is comprised of an electro-conductive layer formed at least on one of the surfaces of said insulation film.

4. The semiconductor device of claim 1, wherein

said insulation member is comprised of an insulation resin, and
said electro-conductive member is comprised of an electro-conductive foil buried in said insulation resin.

5. The semiconductor device of either one of claim 1, claim 2, claim 3 or claim 4, wherein

said coupling member is comprised of a metal extrusion.

6. The semiconductor device of either one of claim 1, claim 2, claim 3 or claim 4, wherein

said electro-conductive member is coupled with at least one of ground terminals of said first semiconductor chip, said second semiconductor chip or an external circuit.

7. A semiconductor device manufacturing method comprising:

a process for disposing a first semiconductor chip having a first electrode pad and a first wiring layer on the main surface and a second semiconductor chip having a second electrode pad and a second wiring layer on the main surface, with respective main surface facing to each other;
a process for disposing an insulation member between said main surfaces, facing to each other, of said first semiconductor chip and said second semiconductor chip;
a process for disposing an electro-conductive member between said main surfaces, facing to each other, of said first semiconductor chip and said second semiconductor chip; and
a process for electrically coupling said first electrode pad and said second electrode pad together with a coupling member.

8. The semiconductor device manufacturing method of claim 7, wherein

said process for disposing an insulation member is comprised of a process to form an insulation layer on at least one of said wiring layers of either said first semiconductor chip or said second semiconductor chip, and
said process for disposing an electro-conductive member is comprised of a process to form an electro-conductive layer on said insulation layer.

9. The semiconductor device manufacturing method of claim 7, wherein

said coupling process is comprised of a process to couple via an extruded electrode formed on both surfaces of an insulation film;
said process for disposing an electro-conductive member is comprised of a process to form an electro-conductive layer on at least one of the surfaces of said insulation film in an area excluding at least said extruded electrode; and
said process for disposing an insulation member is comprised of a process to apply an insulation resin on said first semiconductor chip, a process to place said insulation film on said insulation resin so that said first electrode pad comes to said extruded electrode and said second electrode pad to said extruded electrode, respectively facing to each other, and a process to further apply an insulation resin on said insulation film.

10. The semiconductor device manufacturing method of claim 7, wherein

said process for disposing an insulation member and said process for disposing electro-conductive member are comprised of a process to apply an insulation resin on an area of said first semiconductor chip, a process to place an electro-conductive film on said insulation resin covering an area excluding said first electrode pad, and a process to bury said electro-conductive foil in said insulation resin by applying an insulation resin on said electro-conductive foil.

11. The semiconductor device manufacturing method of either one of claim 7 or claim 8, wherein

said process for disposing an electro-conductive member is comprised of a process to form said electro-conductive member by means of electroless plating.

12. The semiconductor device manufacturing method of either one of claim 7, claim 8, claim 9 or claim 10, further comprising

a process for connecting said electro-conductive member with at least one of the ground terminals of said first semiconductor chip, said second semiconductor chip or an external circuit.

13. A semiconductor device comprising a first semiconductor chip having a first electrode pad, a first wiring layer and a first elements region in the main surface, and a second semiconductor chip having a second electrode pad located at a corresponding place, a second wiring layer and a second elements region in the main surface facing to said first semiconductor chip, wherein

said second semiconductor chip has a square measure larger than that of said first semiconductor chip, and said second wiring layer and said second elements region are formed on said second semiconductor chip in an area away from an area facing to said first wiring layer and said first elements region.

14. The semiconductor device of claim 13, wherein

a memory with which an information is erasable and rewritable by irradiating ultraviolet rays is formed in said second elements region.

15. The semiconductor device of claim 13, wherein

the number of said second electrode pads is more than said first electrode pad counts, and the area of said second elements region is smaller than the square measure of said second semiconductor chip minus the total of said first wiring layer area and said first elements region area.

16. A semiconductor device comprising a first semiconductor chip having a first electrode pad, a first wiring layer and a first elements region in the main surface, and a second semiconductor chip having a second electrode pad located at a corresponding place, a second wiring layer and a second elements region in the main surface facing to said first semiconductor chip, wherein

said first semiconductor chip and said second semiconductor chip are disposed so as said wiring of first wiring layer and wiring of second wiring layer cross to each other at a certain optional angle without having mutual contact.

17. A semiconductor device comprising a first semiconductor chip having a first electrode pad, a first wiring layer and a first elements region in the main surface, and a second semiconductor chip having a second electrode pad located at a corresponding place, a second wiring layer and a second elements region in the main surface facing to said first semiconductor chip, wherein

difference between driving voltage of said first semiconductor chip and driving voltage of said second semiconductor chip is smaller than threshold voltage that determines the ON or OFF of either semiconductor chip among the two chips the driving voltage of which is lower.

FIG. 1

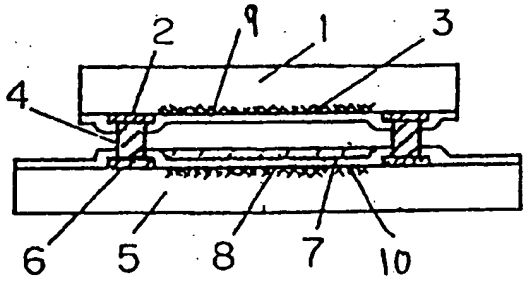

FIG. 2

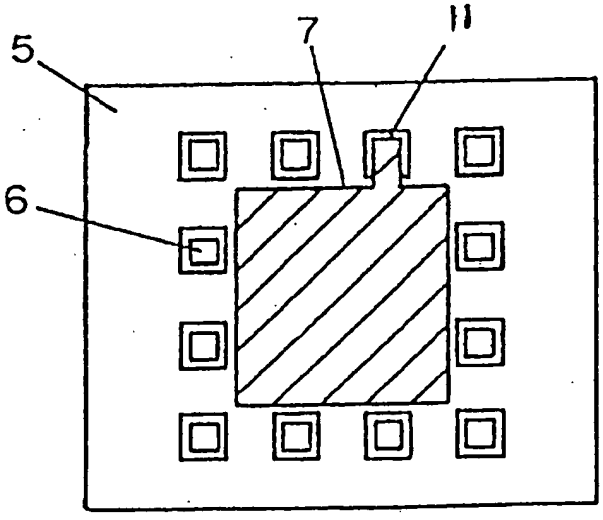

FIG. 3

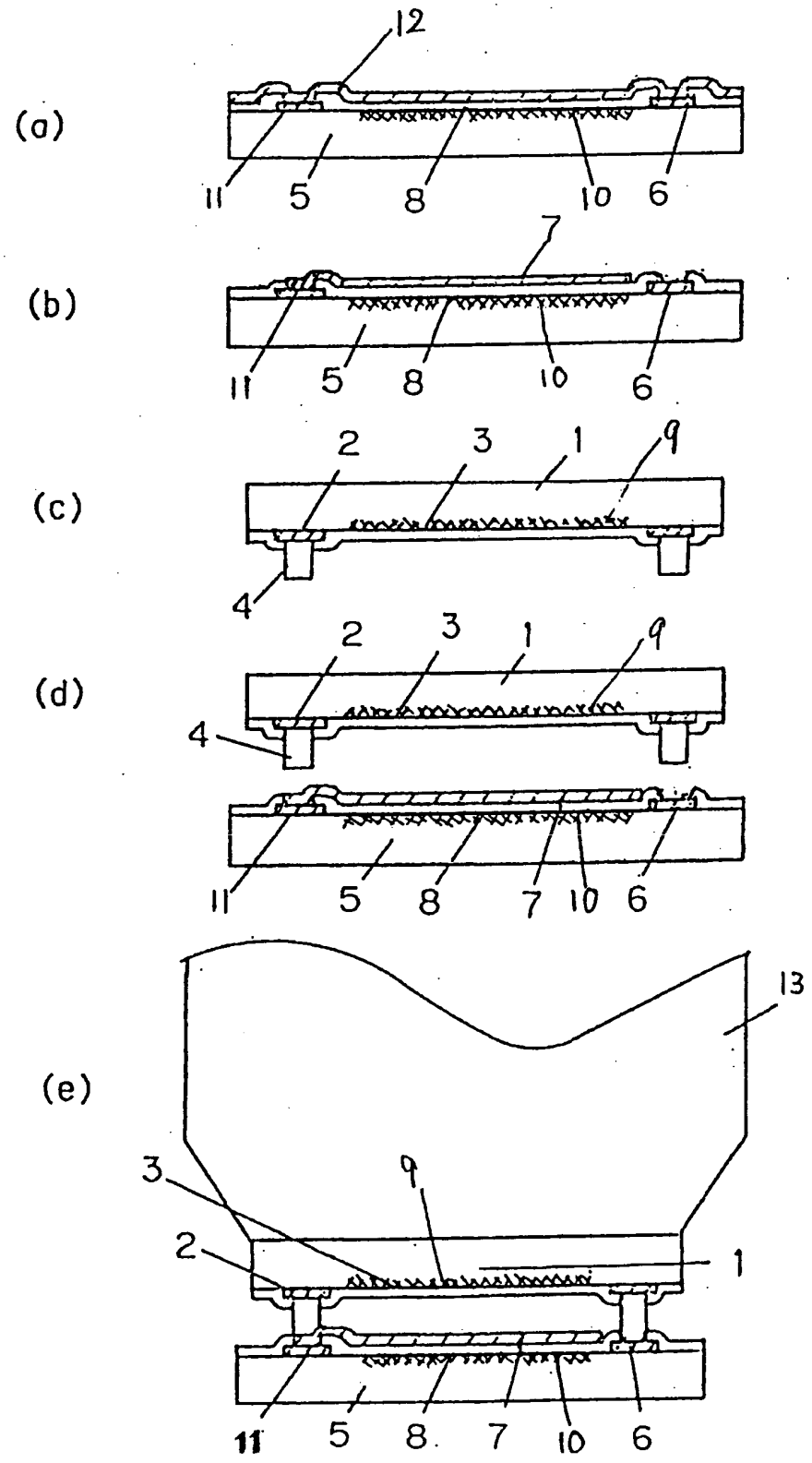
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FIG. 4

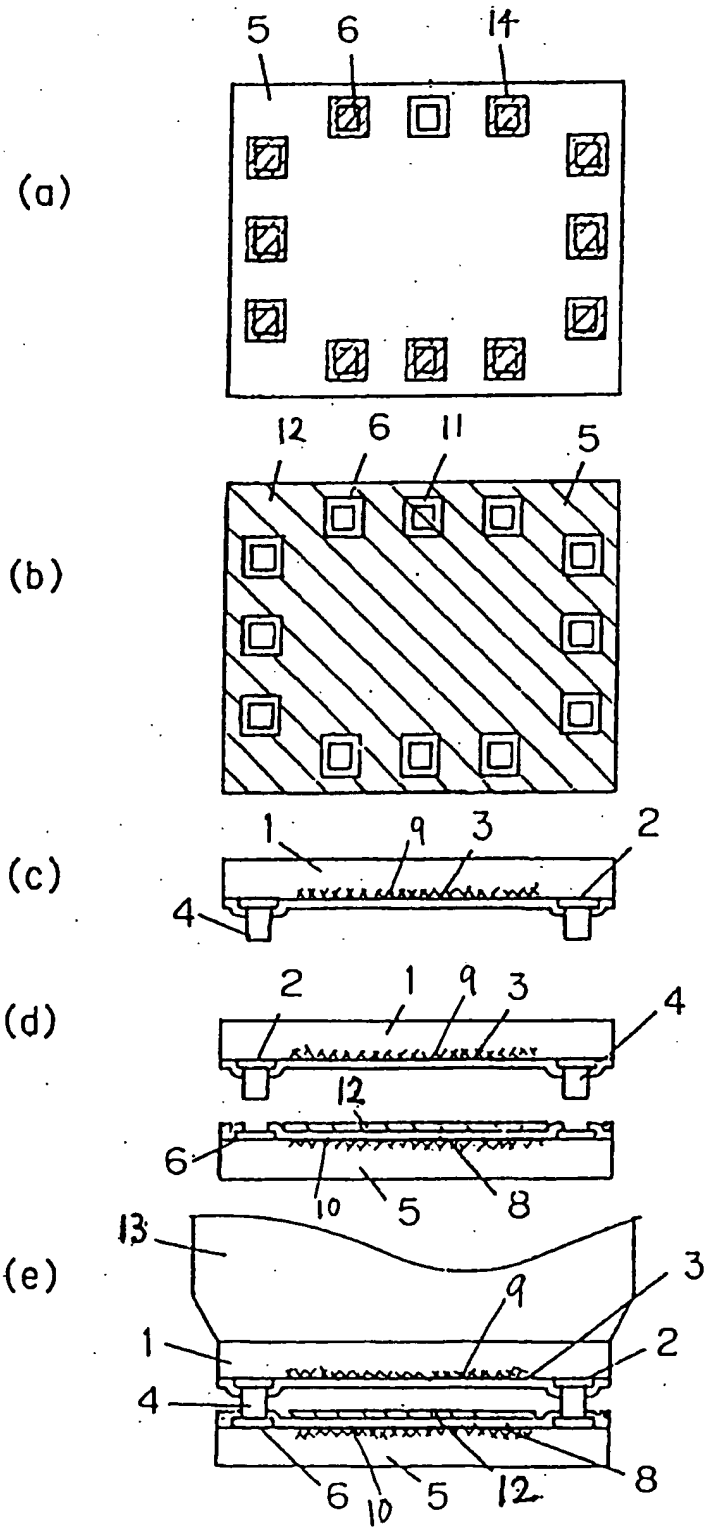

FIG. 5

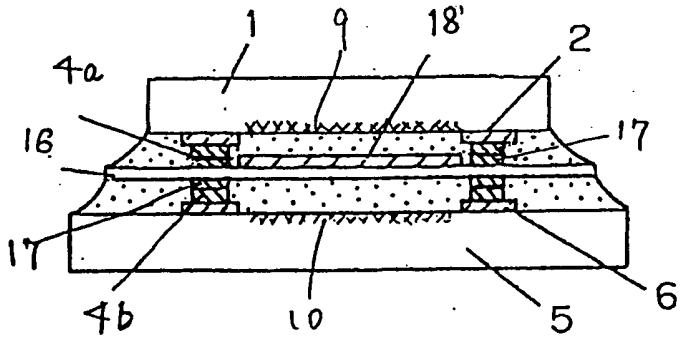

FIG. 6

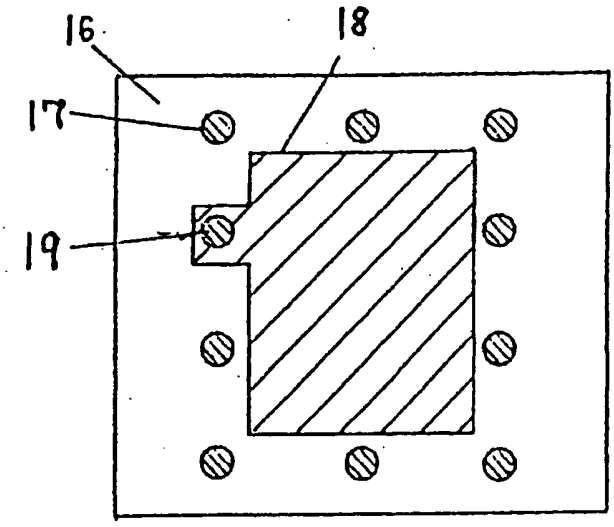

FIG. 7

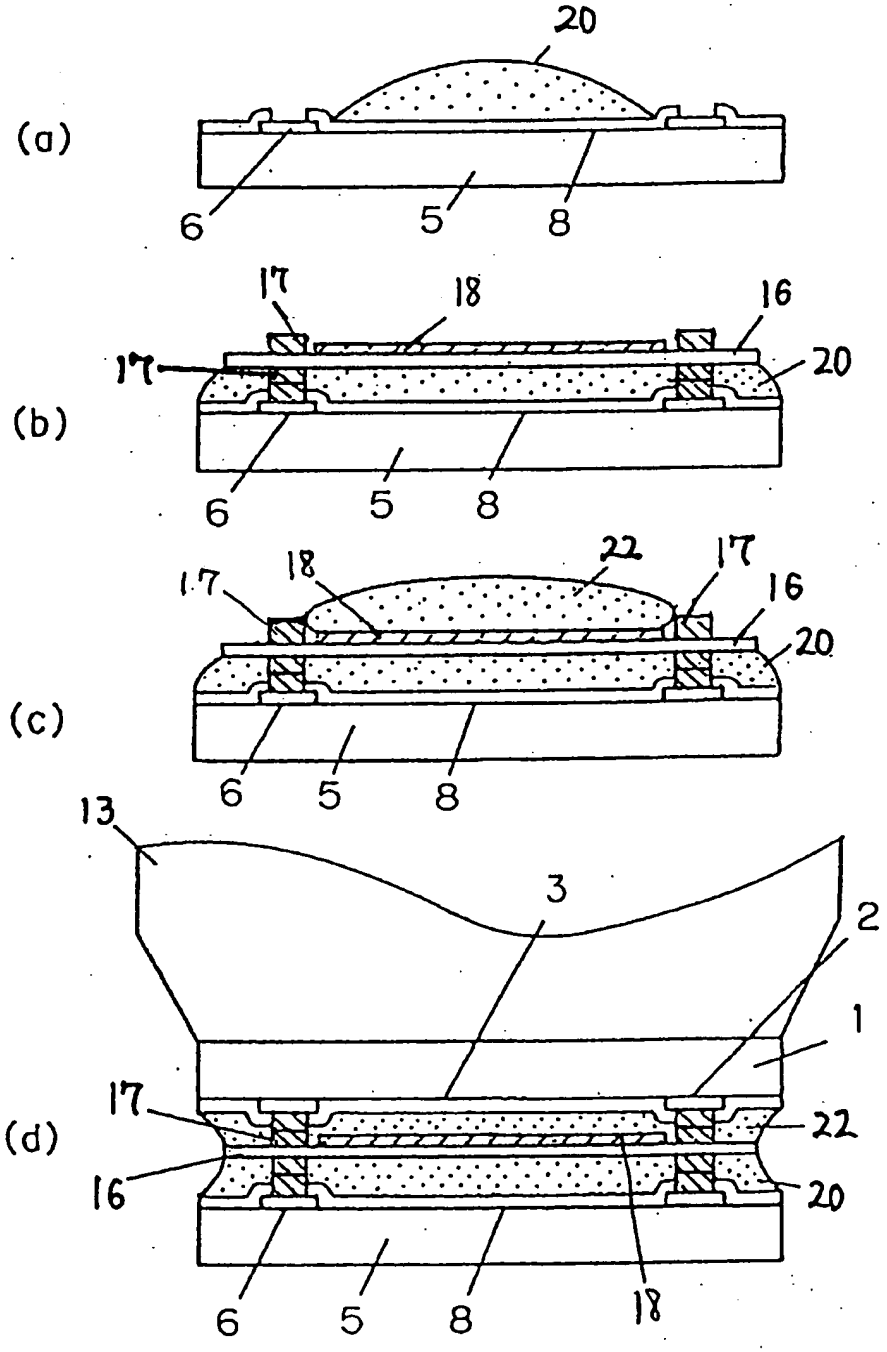
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FIG. 8

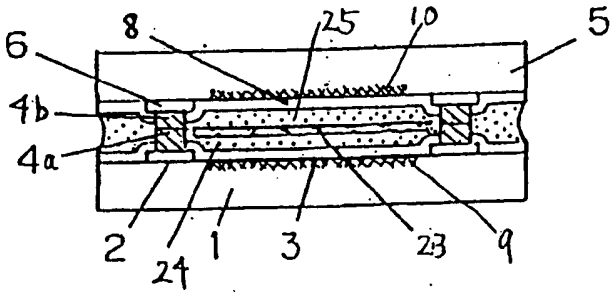
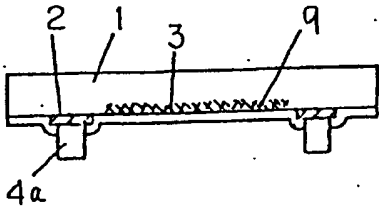


FIG. 9

(a)



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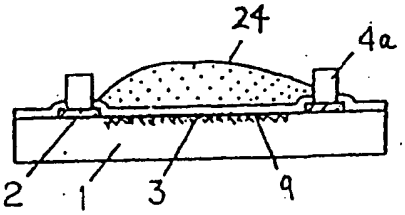

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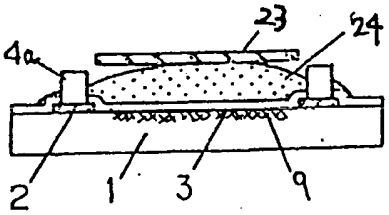

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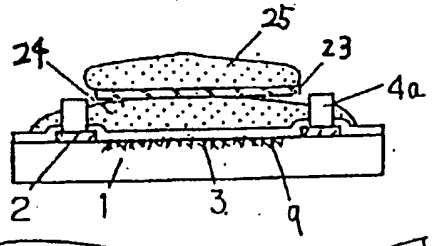

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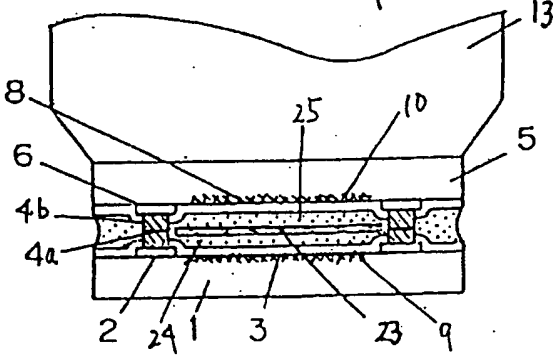

FIG. 10

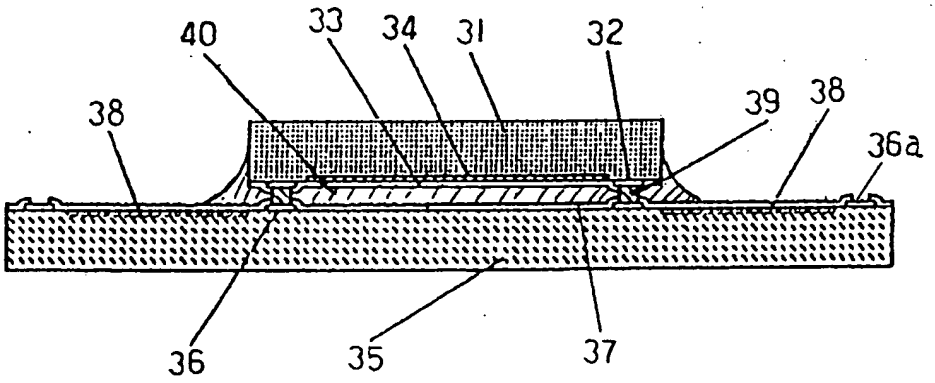

FIG. 11

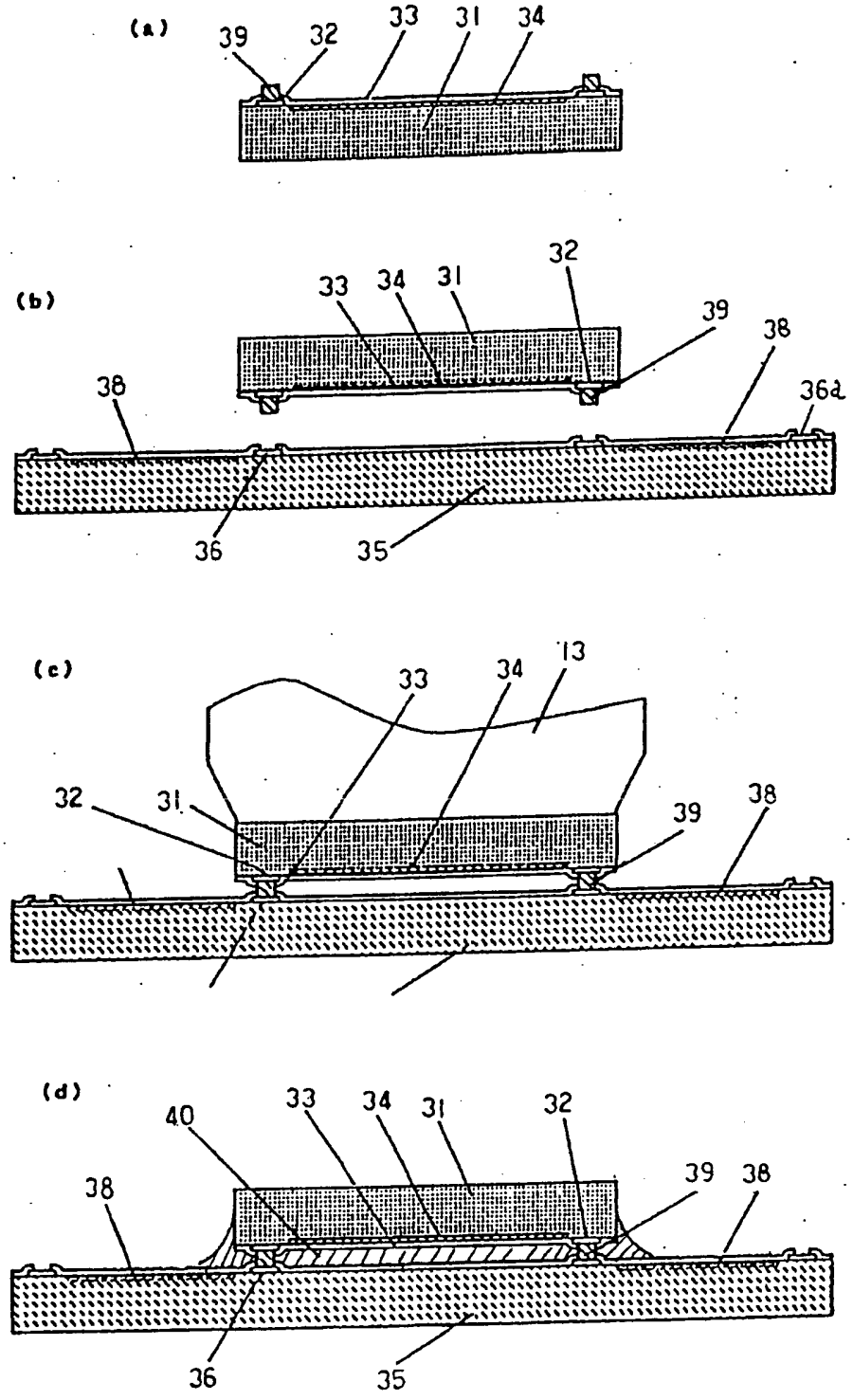
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FIG. 12

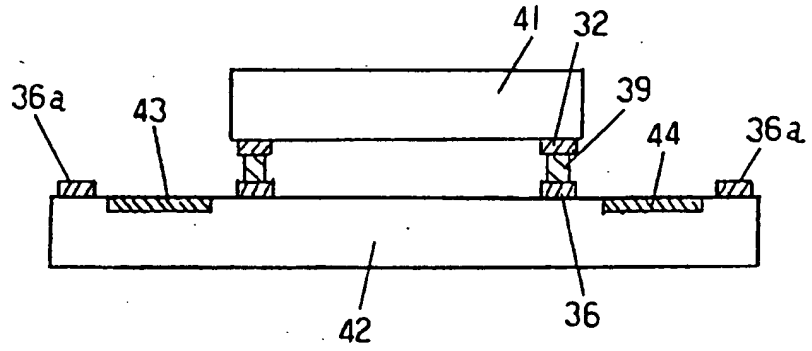


FIG. 13

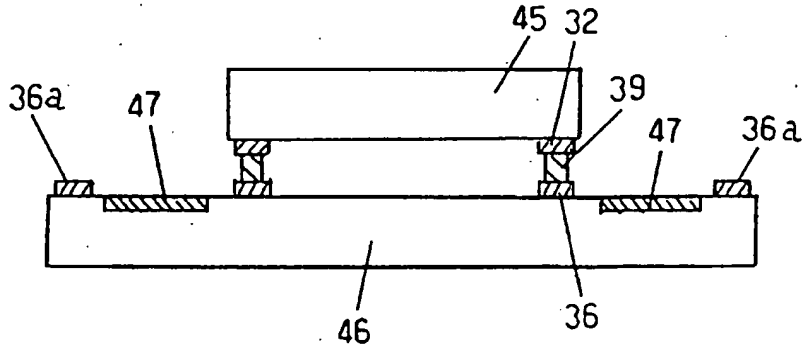


FIG. 14

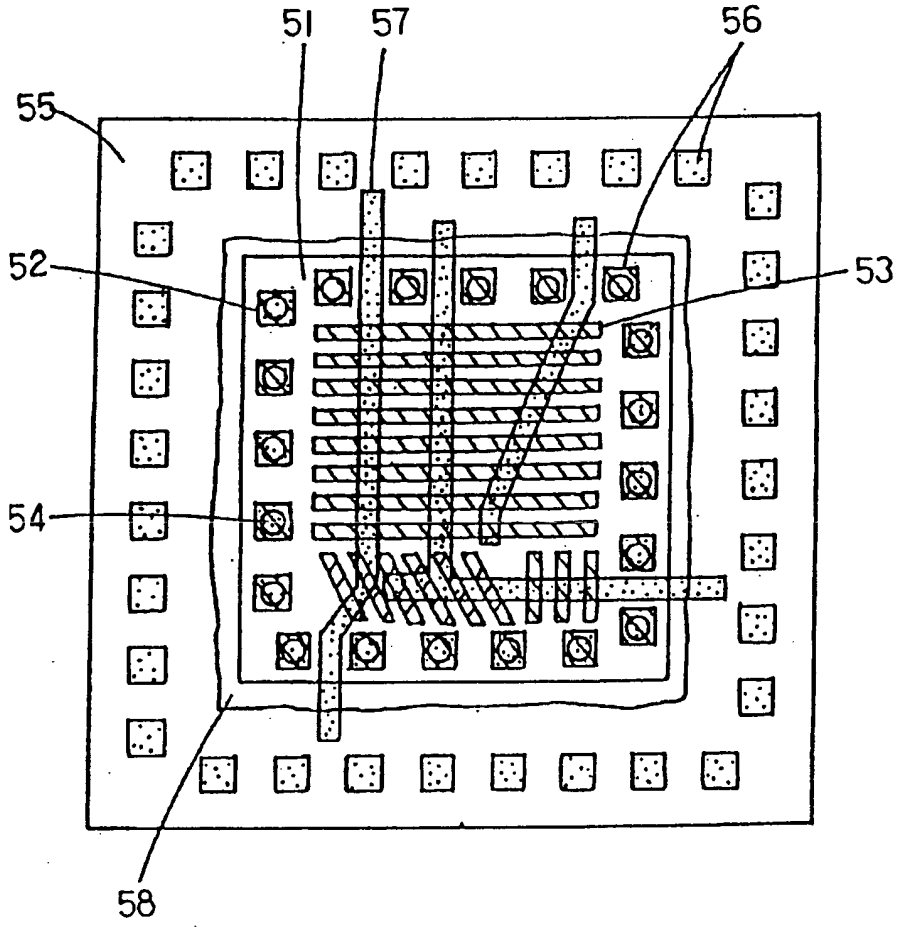


FIG. 15 (a)

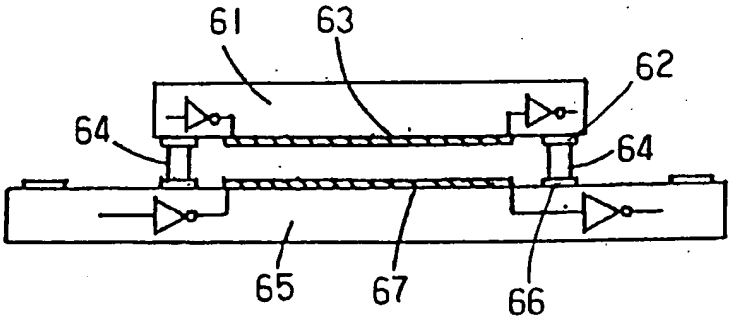


FIG. 15 (b)

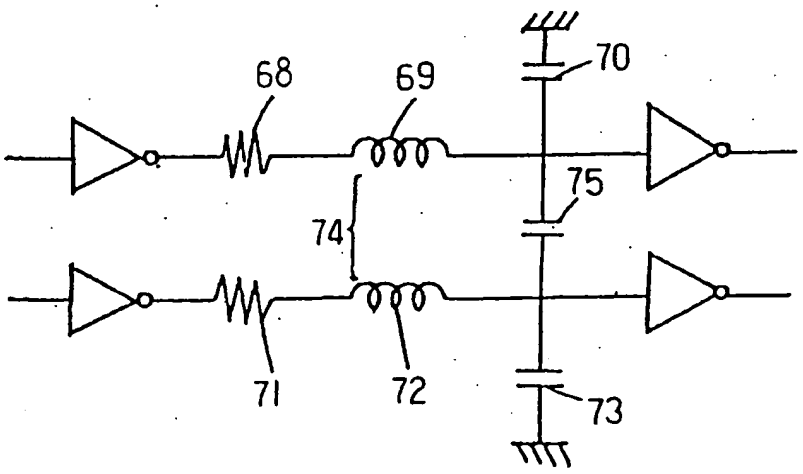
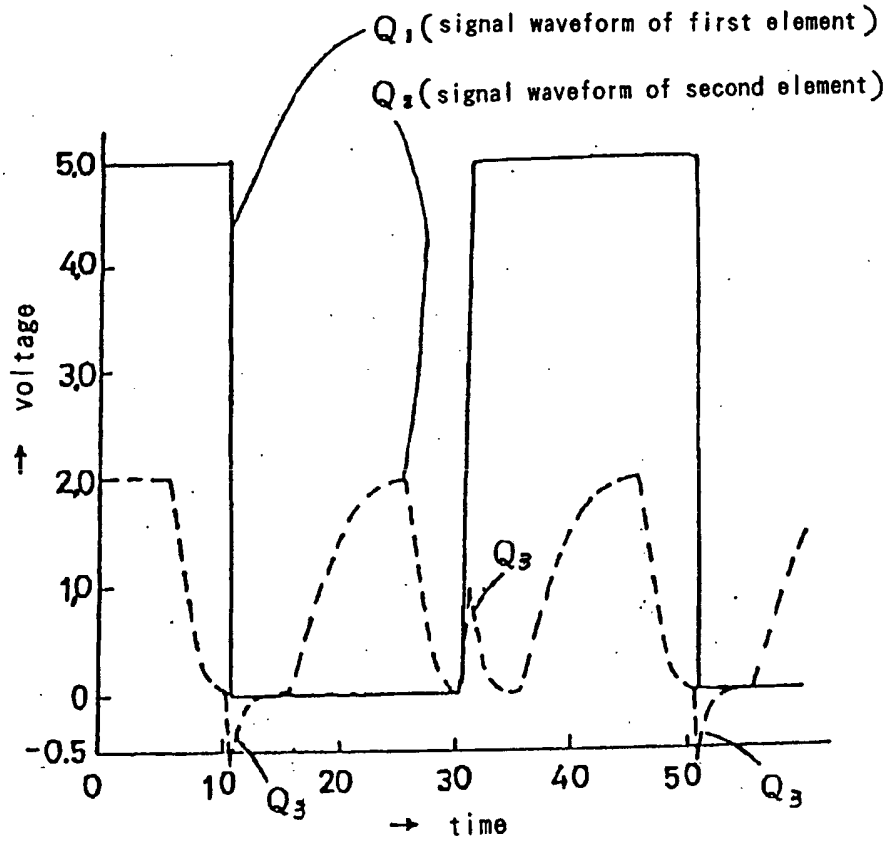


FIG. 16


Q1 (signal waveform of first element)
Q2 (signal waveform of second element)
5.0
4.0
3.0
2.0
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voltage
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time
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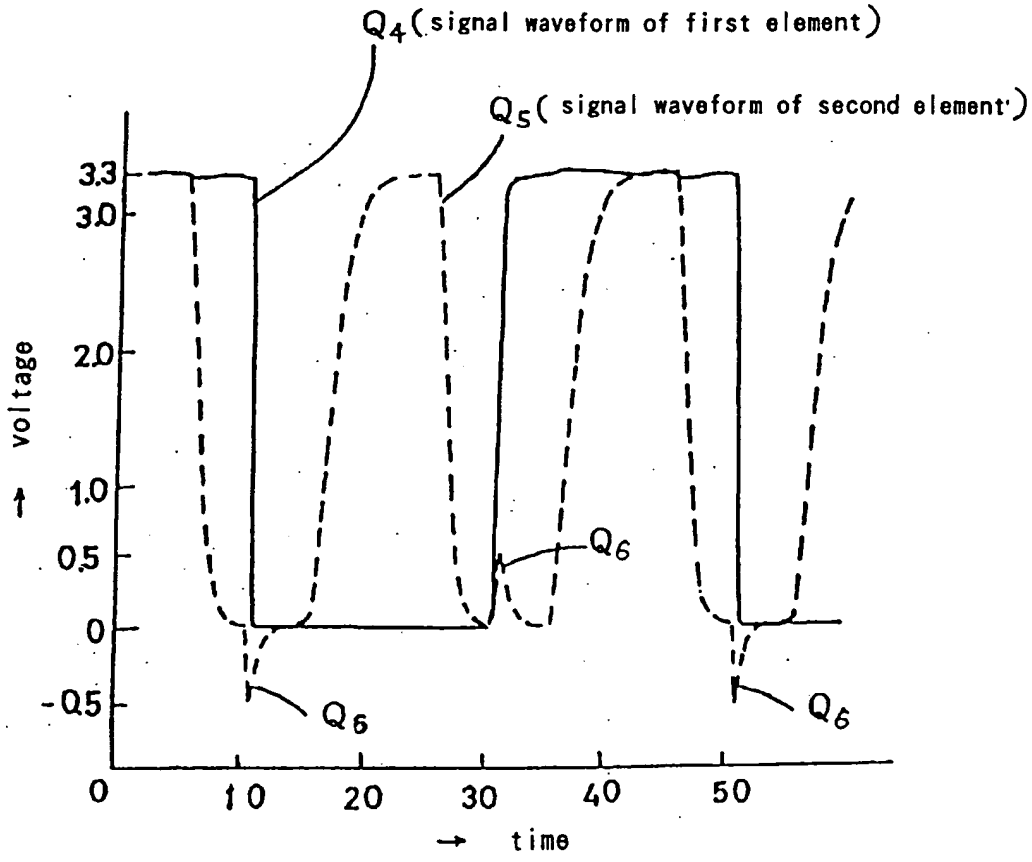
Q3
Q3

FIG. 17


Q4(signal waveform of first element)
Q5(signal waveform of second element)
3.3
3.0
2.0
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0
-0.5
voltage
Q6
Q6
Q6
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30
40
50
time

FIG. 18

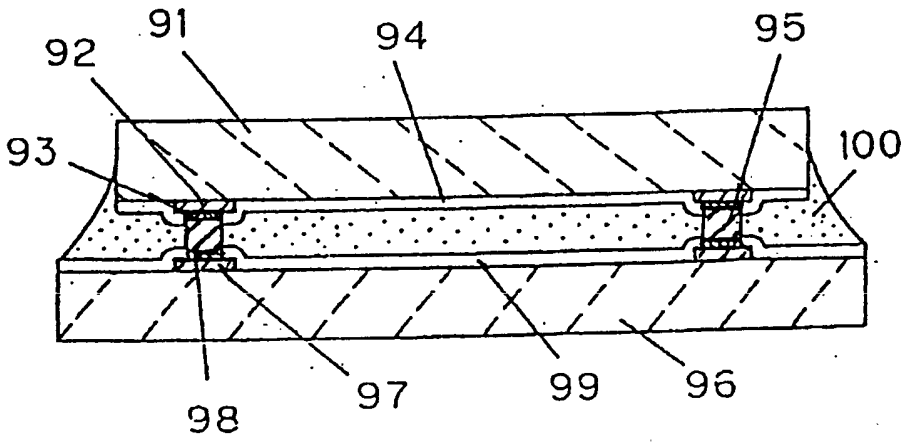
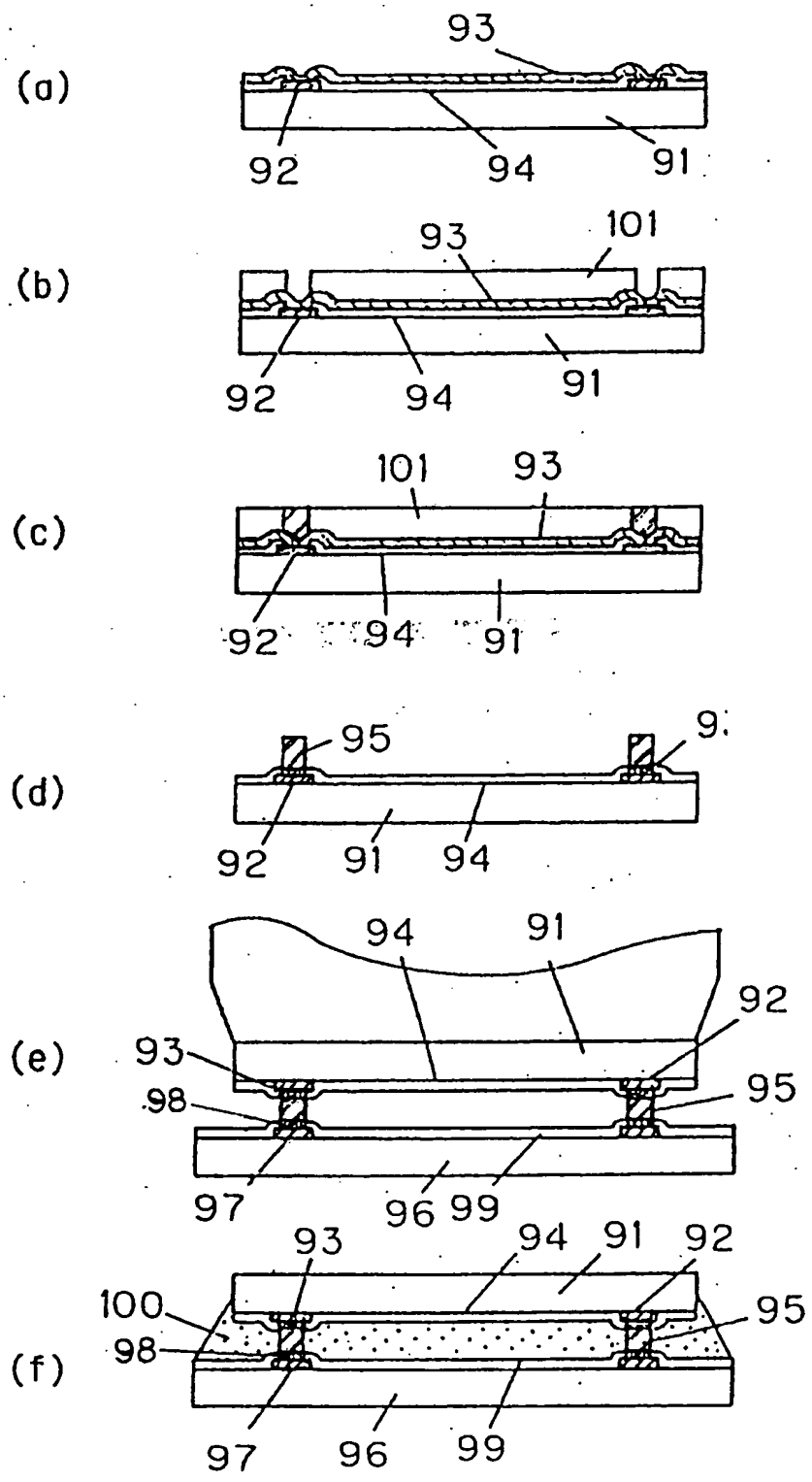


FIG. 19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(19) Europäisches Patentamt
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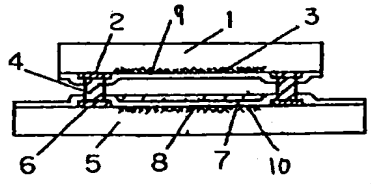
(54) Structure of chip on chip mounting preventing crosstalk noise

(57) The present invention is intended to solve a problem of crosstalk noise in a so-called system module, which occurs as a result of interference between signals running in each of respective wiring layers of a first semiconductor chip and a second semiconductor chip stacked surface to surface with a small gap, and invites malfunctioning of semiconductor devices. As shown in Fig.1, the semiconductor device comprises a first semiconductor chip 1 having a first electrode pad 2 and a first wiring layer 9 in the main surface, a second semiconductor chip 5 having a second electrode pad 6 located at a corresponding place and a second wiring layer 10 in the main surface facing to the first semiconductor chip, a bump 4 for electrically coupling first electrode pad 2 and second electrode pad 6 together, an insulation layer 8 disposed between the main surfaces of first semiconductor chip 1 and second semiconductor chip 5 facing to each other, and an electro-conductive layer 7 disposed between the main surfaces of first semiconductor chip and second semiconductor chip facing to each other.

FIG. 1



EP 0 740 343 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 6001

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	EP 0 348 972 A (SHARP KK) 3 January 1990 (1990-01-03) * column 4, line 45 - column 6, line 23; figures 1,2 *	1-8, 10-12	H01L25/065 H01L23/552 H01L23/522
Y	PATENT ABSTRACTS OF JAPAN vol. 015, no. 026 (E-1025), 22 January 1991 (1991-01-22) -& JP 02 271656 A (MITSUBISHI ELECTRIC CORP), 6 November 1990 (1990-11-06) * abstract *	1-8, 10-12	
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Y	DE 29 02 002 A (KRAUSE GERHARD) 31 July 1980 (1980-07-31) * page 1, paragraph 1 * * page 16, paragraphs 1,2 *	1-8, 10-12	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	EP 0 527 044 A (IBM) 10 February 1993 (1993-02-10) * figures 1-3 *	1-12	
A	US 4 818 728 A (RAI AKITERU ET AL) 4 April 1989 (1989-04-04) * figure 4 *	1-12	
Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 235 (E-275), 27 October 1984 (1984-10-27) & JP 59 117259 A (HITACHI SEISAKUSHO KK;OTHERS: 01), 6 July 1984 (1984-07-06) * abstract *	16	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	20 December 1999	Edmeades, M

CATEGORY OF CITED DOCUMENTS

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& : member of the same patent family, corresponding document

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 6001

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 038 (E-878), 24 January 1990 (1990-01-24) & JP 01 272149 A (HITACHI LTD), 31 October 1989 (1989-10-31) * abstract *	16	
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 248 (E-0933), 28 May 1990 (1990-05-28) & JP 02 071552 A (HITACHI LTD), 12 March 1990 (1990-03-12) * abstract *	13	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	20 December 1999	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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O : non-written disclosure
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D : document cited in the application
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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 96 10 6001

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

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European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 96 10 6001

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-11

   Prevention of crosstalk between first and second opposed chips by an electrically conductive screening member placed in between the chips

2. Claims: 13-15,16

   Prevention of crosstalk between first and second opposed chips by appropriate placement of the wiring layers thereon (providing wiring areas on the second chip in areas remote from the wiring areas of the first chip prevention or forming the wiring layers on each chip to cross at approximately right angles).

3. Claim : 17

   Prevention of crosstalk between first and second opposed chips by appropriate selection of the chip driving voltages.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 96 10 6001

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20-12-1999

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